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**MSPM’S**

**Deogiri Institute of Engineering and Management Studies,**

**Aurangabad.**

**Department of Computer Science and Engineering**

Survey Based On

**Xiaomi Redmi Note 7**

Report Based On

**Manufactures of Processor**

**Subject: Computer Architecture and Organization**

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**CERTIFICATE**

This is to Certify that’s **Mrs. Rani Pawar, Renuka Deolalikar, Pratik Kulkarni** had Successfully Completed

his Survey Based Redmi Note 7 Pro Report on Manufactures of Processor on date 23 /09 /2019 .

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**ABSTRACT**

*This survey base project is about the smartphone made by Xiaomi. For the smartphone made by Samsung, see*[*Samsung Galaxy Note 7*](https://en.wikipedia.org/wiki/Samsung_Galaxy_Note_7)*.* ***Redmi Note 7****refer to a series of smartphones released by*[*Redmi*](https://en.wikipedia.org/wiki/Redmi)*, a sub-brand of*[*Xiaomi*](https://en.wikipedia.org/wiki/Xiaomi)*. Most variants of the phone feature a 48MP camera sensor.The Redmi Note 7 variant comes with a*[*Qualcomm Snapdragon*](https://en.wikipedia.org/wiki/Qualcomm_Snapdragon)*660 CPU while the Redmi Note 7 Pro contains an upgraded*[*Qualcomm Snapdragon*](https://en.wikipedia.org/wiki/Qualcomm_Snapdragon)*675 processor.*

*In August 2019, Xiaomi announced the Redmi Note 7 series has sold more than 20 million units worldwide. Redmi phones use the Xiaomi*[*MIUI*](https://en.wikipedia.org/wiki/MIUI)*user interface on top of*[*Android*](https://en.wikipedia.org/wiki/Android_(operating_system))*. Models can be divided into regular Redmi phones with screens usually up to 5" and Redmi Note series with displays exceeding 5". The only other line is the*[*Redmi Pro*](https://en.wikipedia.org/wiki/Xiaomi#Other_devices)*series, first introduced in 2016 with a dual camera system, USB-C and an*[*OLED*](https://en.wikipedia.org/wiki/AMOLED)*display. The Redmi A series has been marketed in several Asian and European countries. The most significant difference from other Xiaomi smartphones is that they use less-expensive components and thus are more cost-effective. In August 2014,*[*The Wall Street Journal*](https://en.wikipedia.org/wiki/The_Wall_Street_Journal)*reported that in the second quarter of the 2014 fiscal year, Xiaomi had a market share of 14% of smartphone shipment rankings in China. Redmi sales were attributed as a contributing factor toward this gain in shipment rankings.*

1. **XIAOMI REDMI NOTE 7 PRO DESCRIPTION**

**Overview**

The Xiaomi Redmi Note 7 Pro is a mid-range budget smartphone. The phone has good performance well. The smartphone comes with a huge storage space for storing large amount of data or files. It is very good for clicking good images and videos. But the phone comes with a hybrid slot, which is not preferred by many users. The phone offers a truly immersive and enriched smartphone experience. Powered by a 2.0 GHz Qualcomm Snapdragon 675 processor and a dual (48 MP + 5 MP) rear camera the phone has everything you need. It also has Face Unlock feature which makes unlocking the phone a piece of cake, and provides additional security.The phone has a 13 MP front camera comes with features such as AI Beautify 4.0 and AI Portrait mode which let you take beautiful bokeh selfies easily

## **1.2 INTRODUCTION**

On 10 January 2019, Xiaomi unveiled the Redmi Note 7 and Redmi Note 7 Pro. The Redmi Note 7 and Redmi Note 7 Pro are the first phones in the Redmi series to feature a 48-megapixel rear camera. However, the Redmi Note 7 features a Samsung GM1 sensor and the Redmi Note 7 Pro features a Sony IMX586 48MP sensor. The Redmi Note 7 is powered by the Qualcomm Snapdragon 660 Octa-Core Processor clocked at 2.2GHz, while the Redmi Note 7 Pro features an 11nm Qualcomm Snapdragon 675 Octa-Core Processor clocked at 2.0GHz. Since then, Redmi became a sub-brand separated from Xiaomi.

On March 20, 2019 the Redmi Note 7 launched in the Philippines; it runs on the Qualcomm Snapdragon 660 AIE 2.2GHZ SoC along with the Adreno 512 GPU. It has three variants: 3GB RAM with 32GB storage, 4GB RAM with 64GB storage and 6GB RAM with 64GB storage. It has a 4,000mAh battery with QuickCharge 4.0. The Redmi Note 7 series of smartphones is one of the bestselling phone by Redmi. Company has announced, that sold [over 20 millions devices](https://vosveteit.sk/predaje-redmi-note-7-serie-smartfonov-prekrocili-magicku-hranicu/) in 7 month from introduction of phone.

The **Redmi Note 7 Pro** includes a 6.3-inch full HD+ (2340x1080 pixels) display with a 19.5:9 aspect ratio. It is powered by an 11nm Octa-Core Snapdragon 675 processor, making it the first **Xiaomi** device to use the chip. The device runs on Adreno 612 GPU and a 4000 mAh battery.

**Codename:** Redmi Note 7: lavender; Redmi N...

**Series:** [Xiaomi Redmi](https://en.wikipedia.org/wiki/Xiaomi_Redmi)

**Predecessor:** [Redmi Note 5](https://en.wikipedia.org/wiki/Redmi_Note_5); [Redmi Note 6 Pro](https://en.wikipedia.org/wiki/Redmi_Note_6_Pro)

**Successor:** [Redmi Note 8](https://en.wikipedia.org/wiki/Redmi_Note_8)

Redmi Note 7 refer to a series of smartphones released by [Redmi](https://en.wikipedia.org/wiki/Redmi), a sub-brand of [Xiaomi](https://en.wikipedia.org/wiki/Xiaomi). Most variants of the phone feature a 48MP camera sensor. The Redmi Note 7 variant comes with a [Qualcomm Snapdragon](https://en.wikipedia.org/wiki/Qualcomm_Snapdragon) 660 CPU while the Redmi Note 7 Pro contains an upgraded [Qualcomm Snapdragon](https://en.wikipedia.org/wiki/Qualcomm_Snapdragon) 675 processor.



**1.1 Redmi note 7 Pro**

**1.3 Redmi Note 7 Pro Summary**

The Redmi Note 7 Pro is one of the most feature packed phones in its price bracket, bringing a premium design, capable octa-core processor, 48-megapixel camera, and fast charging support to the table. The phone packs a 6.3-inch full-HD+ (1080x2340 pixels) LTPS In-Cell display protected by a layer of Gorilla Glass 5. Content on the display looks sharp with crisp colours, but at the same time, it is also quite reflective.

The phone is powered by the Snapdragon 675 processor ticking alongside up to 6GB of RAM. Be it heavy multitasking or games like PUBG Mobile and Asphalt 9, the phone barely struggles at all. The Redmi Note 7 Pro runs MIUI 10 based on Android 9 Pie, and even though it is rich in features, you will also have to see pesky ads.

The phone’s 48-megapixel main camera captures beautiful images with ample detail, high dynamic range, and good vibrancy. The night mode also performs well, while selfies captured by the 32-megapixel front camera also look sharp with natural colours and edge detection in bokeh mode. The 4,000mAh battery ensures that the Redmi Note 7 Pro easily sails past a full day of usage, while support for Qualcomm's Quick Charge 4.0 fast charging technology helps to quickly top up the battery.

1. **Redmi Note 7 Pro Processor Architecture**

Hardware. The **Redmi Note 7 Pro** includes a 6.3-inch full HD+ (2340x1080 pixels) display with a 19.5:9 aspect ratio. It is powered by an 11nm Octa-Core Snapdragon 675 **processor**, making it the first **Xiaomi** device to use the chip. The device runs on Adreno 612 GPU and a 4000 mAh battery.

**Codename:**Redmi Note 7: lavender; Redmi N...

**Predecessor:**[Redmi Note 5](https://en.wikipedia.org/wiki/Redmi_Note_5); [Redmi Note 6 Pro](https://en.wikipedia.org/wiki/Redmi_Note_6_Pro)

**Rear camera:**Dual: 48MP + 5MP See #Specifi...

**Series:**[Xiaomi Redmi](https://en.wikipedia.org/wiki/Xiaomi_Redmi)

1. **SPECIFICATION**

The Redmi Note 7 Pro features a shiny glass back with a gradient that Xiaomi calls "Aura Design". Both the front and back of the device have 2.5D curved [Gorilla Glass 5](https://en.wikipedia.org/wiki/Gorilla_Glass). The phone also has a P2i nano-coating that makes it splash resistant, nevertheless the Phone hasn't received an official [IP Code](https://en.wikipedia.org/wiki/IP_Code).[[16]](https://en.wikipedia.org/wiki/Redmi_Note_7#cite_note-16) In other markets such as India, available color variants include Nebula Red, Space Black, and Neptune Blue.The Redmi Note 7 Pro also features a waterdrop notch in the display to accommodate the front-facing camera.

|  |  |
| --- | --- |
| Codename | Redmi Note 7: lavender Redmi Note 7 Pro: violet |
| [Manufacturer](https://en.wikipedia.org/wiki/List_of_mobile_phone_makers_by_country) | [Redmi](https://en.wikipedia.org/wiki/Redmi) |
| [Slogan](https://en.wikipedia.org/wiki/Slogan) | 48MP Camera Beast |
| Series | [Xiaomi Redmi](https://en.wikipedia.org/wiki/Xiaomi_Redmi) |
| Predecessor | [Redmi Note 5](https://en.wikipedia.org/wiki/Redmi_Note_5) [Redmi Note 6 Pro](https://en.wikipedia.org/wiki/Redmi_Note_6_Pro) |
| Successor | [Redmi Note 8](https://en.wikipedia.org/wiki/Redmi_Note_8) |
| Related | Redmi 7 |
| Type | [Touchscreen](https://en.wikipedia.org/wiki/Touchscreen) [smartphone](https://en.wikipedia.org/wiki/Smartphone) |
| [Form factor](https://en.wikipedia.org/wiki/Form_factor_(mobile_phones)) | [Slate phone](https://en.wikipedia.org/wiki/Slate_phone) |
| Dimensions | H: 159.2 mm (6.27 in) W: 75.2 mm (2.96 in) D: 8.1 mm (0.32 in) |
| Mass | 186 g (6.6 oz) |
| [Operating system](https://en.wikipedia.org/wiki/Mobile_operating_system) | [MIUI 10](https://en.wikipedia.org/wiki/MIUI) based on [Android](https://en.wikipedia.org/wiki/Android_(operating_system))[Pie](https://en.wikipedia.org/wiki/Android_Pie) |
| Data inputs | Sensors:   * [Accelerometer](https://en.wikipedia.org/wiki/Accelerometer) * [Gyroscope](https://en.wikipedia.org/wiki/Gyroscope) * [Fingerprint scanner](https://en.wikipedia.org/wiki/Fingerprint_scanner) (rear-mounted) * [Proximity sensor](https://en.wikipedia.org/wiki/Proximity_sensor) * [Electronic compass](https://en.wikipedia.org/wiki/Magnetometer) * [Ambient light sensor](https://en.wikipedia.org/wiki/Ambient_light_sensor) |
| Display | 6.3 inches, 2340 x 1080 pixels, 19.5:9 ratio (403 ppi), LCD capacitive touchscreen, 16M colors |
| Rear camera | Dual: 48[MP](https://en.wikipedia.org/wiki/Megapixel) + 5[MP](https://en.wikipedia.org/wiki/Megapixel) See [#Specifications](https://en.wikipedia.org/wiki/Redmi_Note_7#Specifications), depth sensor, phase detection autofocus, LED flash, Geo-tagging, touch focus, face detection, panorama, HDR |
| Front camera | 13 [MP](https://en.wikipedia.org/wiki/Megapixel) (f/2.0) |
| Connectivity | [USB 2.0](https://en.wikipedia.org/wiki/USB_2.0) [Type-C](https://en.wikipedia.org/wiki/USB-C) 3.5 mm [headphone jack](https://en.wikipedia.org/wiki/Phone_connector_(audio)) [Wi-Fi](https://en.wikipedia.org/wiki/Wi-Fi) [802.11a](https://en.wikipedia.org/wiki/IEEE_802.11)/b/g/n/ac, [WiFi Direct](https://en.wikipedia.org/wiki/WiFi_Direct), MU-MIMO, Dual-band simultaneous (DBS), Integrated baseband, [LTE](https://en.wikipedia.org/wiki/LTE_(telecommunication))/[Wi-Fi](https://en.wikipedia.org/wiki/Wi-Fi) antenna sharing [Bluetooth](https://en.wikipedia.org/wiki/Bluetooth) V5, [A2DP](https://en.wikipedia.org/wiki/A2DP), Low-energy |

**4.DESIGN**

The Redmi Note 7 Pro features a shiny glass back with a gradient that Xiaomi calls "Aura Design"Both the front and back of the device have 2.5D curved [Gorilla Glass 5](https://en.wikipedia.org/wiki/Gorilla_Glass). The phone also has a P2i nano-coating that makes it splash resistant, nevertheless the Phone hasn't received an official [IP Code](https://en.wikipedia.org/wiki/IP_Code).[[16]](https://en.wikipedia.org/wiki/Redmi_Note_7#cite_note-16) In other markets such as India, available colour variants include Nebula Red, Space Black, and Neptune Blue

|  |  |
| --- | --- |
| **Screen size (inches)** | 6.30 |
| **Touchscreen** | Yes |
| **Resolution** | 1080x2340 pixels |
| **Protection type** | Gorilla Glass |
| **Aspect ratio** | 19.5:9 |
| **Pixels per inch (PPI)** | 409 |
| **Touchscreen type** | Capacitive, Multitouch |
| **Color Reproduction** | 16M Colors |
| **Protection** | Corning Gorilla Glass 5 |
| **Screen to body percentage** | 81.4% |





**Display**

**5.HARDWARE**

The Redmi Note 7 Pro includes a 6.3-inch full HD+ (2340x1080 pixels) display with a 19.5:9 aspect ratio. It is powered by an [11nm](https://en.wikipedia.org/wiki/11_nanometer)[[2]](https://en.wikipedia.org/wiki/Redmi_Note_7#cite_note-:1-2) Octa-Core Snapdragon 675 processor, makinit the first Xiaomi device to use the chip. The device runs on Adreno 612 GPU and a 4000 [mAh](https://en.wikipedia.org/wiki/MAh) battery. It also supports Quick Charge 4. It comes with either 4GB RAM with 64GB storage or 6GB RAM with 128GB storage; storage is expandable up to 256 GB. Sony IMX586 sensor with f/1.8 aperture along with a secondary 5 megapixel depth sensor. The selfie camera has 13 megapixels. The rear camera is capable of recording 4K videos at 30fps.

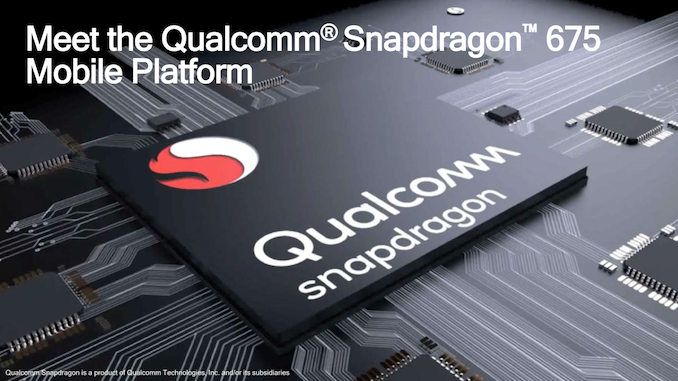
The Redmi Note 7 Pro has a studio lighting mode live option as well. The feature shows what studio lighting effect will look like. The phone has AI scene detection capable of recognizing up to 12 scenes,[[3]](https://en.wikipedia.org/wiki/Redmi_Note_7#cite_note-:3-3) AI Portrait 2.0 and a Night Mode as well.

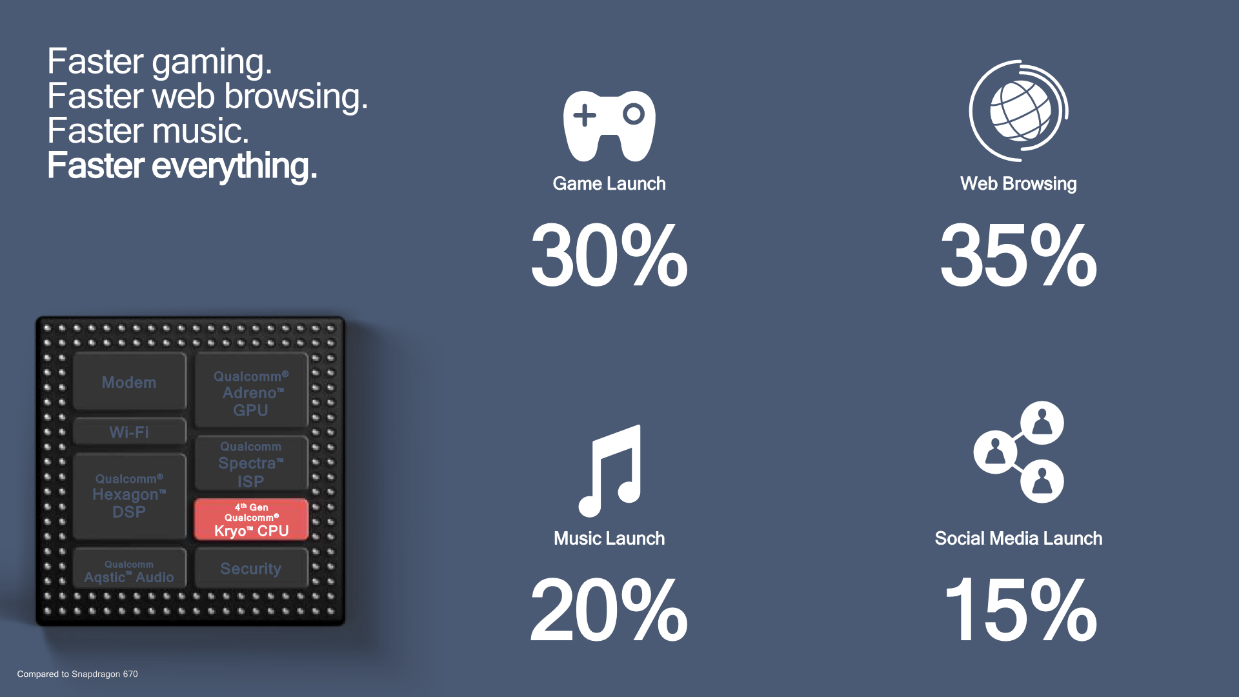
### Connectivity

|  |  |
| --- | --- |
| **Processor** | 2GHz octa-core |
| **Processor make** | Qualcomm Snapdragon 675 |
| **RAM** | 4GB |
| **Internal storage** | 64GB |
| **Expandable storage** | Yes |
| **Expandable storage type** | microSD |

**Processor:**

Snapdragon 675 is amid-range [64-bit](https://en.wikichip.org/wiki/64-bit_architecture) [ARM](https://en.wikichip.org/wiki/ARM) [LTE](https://en.wikichip.org/wiki/LTE) [system on a chip](https://en.wikichip.org/w/index.php?title=system_on_a_chip&action=edit&redlink=1) designed by [Qualcomm](https://en.wikichip.org/wiki/Qualcomm) and introduced in late [2018](https://en.wikichip.org/wiki/2018). Fabricated on Samsung's [11nm LPP process](https://en.wikichip.org/wiki/11_nm_process), the 675 features six [Kryo 460 Silver](https://en.wikichip.org/wiki/Kryo_460_Silver) high-efficiency cores operating at 1.8 GHz along with two high-performance [Kryo 460 Gold](https://en.wikichip.org/wiki/Kryo_460_Gold) operating at 2 GHz. The Snapdragon 675 integrates the [Adreno 612](https://en.wikichip.org/w/index.php?title=qualcomm/adreno_612&action=edit&redlink=1) [GPU](https://en.wikichip.org/w/index.php?title=GPU&action=edit&redlink=1) and features an X12 LTE modem supporting Cat 13 uplink and Cat 15 downlink. This chip supports up to 8 GiB of dual-channel LPDDR4X-3733 memory.





|  |  |
| --- | --- |
| **Snapdragon 675** | |
| **General Info** | |
| **Designer** | [Qualcomm](https://en.wikichip.org/wiki/Qualcomm), [ARM Holdings](https://en.wikichip.org/wiki/ARM_Holdings) |
| **Manufacturer** | [Samsung](https://en.wikichip.org/wiki/Samsung) |
| **Model Number** | SDM675 |
| **Market** | Mobile |
| **Introduction** | October 22, 2018 (announced) October 22, 2018 (launched) |
| **General Specs** | |
| **Family** | [Snapdragon 600](https://en.wikichip.org/w/index.php?title=qualcomm/snapdragon_600&action=edit&redlink=1) |
| **Frequency** | 2,000 MHz, 1,800 MHz |
| **Microarchitecture** | |
| **ISA** | ARMv8 (ARM) |
| **Microarchitecture** | [Cortex-A76](https://en.wikichip.org/wiki/qualcomm/microarchitectures/cortex-a76), [Cortex-A55](https://en.wikichip.org/wiki/qualcomm/microarchitectures/cortex-a55) |
| **Core Name** | [Kryo 460 Gold](https://en.wikichip.org/wiki/qualcomm/cores/kryo_460_gold), [Kryo 460 Silver](https://en.wikichip.org/wiki/qualcomm/cores/kryo_460_silver) |
| **Process** | [11 nm](https://en.wikichip.org/wiki/11_nm_process) |
| **Technology** | CMOS |
| **Word Size** | 64 bit |
| **Cores** | 8 |
| **Threads** | 8 |
| **Max CPUs** | 1 (Uniprocessor) |
| **Max Memory** | 8 GiB |

**6. Camera**

**Xiaomi Redmi Note 7 Pro Camera Review**

Camera performance has always been a strength of Xiaomi’s affordable phones. Even the last generation Redmi Note 6 is better than most currently available options, so the 48MP Sony IMX576 sensor on the affordable Note 7 Pro takes the game to a whole new level.

The IMX586 is designed to give the best shots in the 12MP mode, where four adjoining pixels are clubbed as one, but you may also shoot in full 48MP resolution using the pro mode or changing camera settings. The 48MP shots aren’t as crisp though, so you’d be better off with 12MP images.

The images shot on the Note 7 Pro in proper lighting look amazing. In tricky lighting, the phone tends to suppress details in the shadow region. The HDR Mode can be a hit or a miss.

|  |  |
| --- | --- |
| **Rear**[**camera**](https://en.wikipedia.org/wiki/Camera_phone) | Dual: 48[MP](https://en.wikipedia.org/wiki/Megapixel) + 5[MP](https://en.wikipedia.org/wiki/Megapixel) See [#Specifications](https://en.wikipedia.org/wiki/Redmi_Note_7#Specifications), depth sensor, phase detection autofocus, LED flash, Geo-tagging, touch focus, face detection, panorama, HDR |
| [**Front camera**](https://en.wikipedia.org/wiki/Front-facing_camera) | 1. [MP](https://en.wikipedia.org/wiki/Megapixel) (f/2.0) |

****

**Fig Camera**

**7. Software**

The Redmi Note 7 runs on Xiaomi's [MIUI](https://en.wikipedia.org/wiki/MIUI) OS V10.3.13.0 currently with august security patch level. It is based on Android Pie(P).Xiaomi has confirmed that this phone will be upgraded to Android 10 by 2020.[[4]](https://en.wikipedia.org/wiki/Redmi_Note_7#cite_note-:4-4)

**Software**

As for the software, there is familiar MIUI 10 software and this time Xiaomi is backing it with the latest Android 9 Pie right at launch. The interface is generously laden with ads but other than that there are ample customization options and plenty to like.

|  |  |
| --- | --- |
| Operating system | Android Pie |
| Skin | MIUI 10 |

**Fig Software**

|  |  |
| --- | --- |
| **8. Sim Slot**  **SIM 1** | |
| SIM Type | Nano-SIM |
| GSM/CDMA | GSM |
| 3G | Yes |
| 4G/ LTE | Yes |
| Supports 4G in India (Band 40) | Yes |
| **SIM 2** | |
| SIM Type | Nano-SIM |
| GSM/CDMA | GSM |
| 3G | Yes |
| 4G/ LTE | Yes |
| Supports 4G in India (Band 40) | Yes |

**Fig . Sim Slot**

**9. Sensors**

|  |  |
| --- | --- |
| Face unlock | Yes |
| Fingerprint sensor | Yes |
| Compass/ Magnetometer | Yes |
| Proximity sensor | Yes |
| Accelerometer | Yes |
| Ambient light sensor | Yes |
| Gyroscope | Yes |

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**10. Xiaomi Redmi Note 7 Pro advantages, disadvantages**

**Xiaomi Redmi Note 7 Pro has IPS LCD capacitive touchscreen, 16M colors, It offers a size of 6.3 inches, 97.4 cm2 (~81.4% screen-to-body ratio) that is suitable for playing games, watching videos & browsing the internet, It has a resolution of 1080 x 2340 pixels, 19.5:9 ratio (~409 ppi density), and it comes with Corning Gorilla Glass 5 for the screen protection.**

**10.1 Xiaomi Redmi Note 7 Pro advantages**

**Xiaomi Redmi Note 7 Pro comes with the latest operating system of Android 9.0 (Pie), MIUI 10, It has Qualcomm SDM675 Snapdragon 675 (11 nm), It offers a fast CPU, It supports Octa-core (2×2.0 GHz Kryo 460 Gold & 6×1.7 GHz Kryo 460 Silver), It includes Adreno 612 and it gives you superb performance without any lags.**

**Xiaomi Redmi Note 7 Pro has superb expandable memory via card slot, microSD, up to 256 GB (uses SIM 2 slot), It offers high internal memory of 128 GB, 6 GB RAM or it presents superb internal memory of 64 GB, it has 4 GB RAM that is very useful in multitasking performance, It offers lots of RAM & large memory.**

**Xiaomi Redmi Note 7 Pro has the main camera of Dual 48 MP, f/1.8, 1/2″, 0.8µm, PDAF, it has 5 MP, f/2.4, depth sensor, It offers features such as Dual-LED flash, HDR, panorama, It takes amazing photos with high quality, and it provides you with a flash that enables you to take superb photos in low light condition.**

**Xiaomi Redmi Note 7 Pro has video of 2160p@30fps, 1080p@30/60/120fps, (gyro-EIS), It offers 4K video recording, It presents a selfie camera of Single 13 MP, It has features such as HDR, It contains video of 1080p@30fps and it gives you amazing selfies.**

**Xiaomi Redmi Note 7 Pro has 2G bands GSM 850 / 900 / 1800 / 1900 – SIM 1 & SIM 2, It presents 3G bands HSDPA 850 / 900 / 1900 / 2100, It presents 4G bands LTE band 1(2100), 3(1800), 5(850), 7(2600), 8(900), 40(2300), 41(2500), Speed is HSPA 42.2/5.76 Mbps, LTE-A (3CA) Cat9 450/50 Mbps, It offers GPRS and it presents EDGE.**

**Xiaomi Redmi Note 7 Pro is announced in 2019, February, It will be released in 2019, March, The body dimensions are 159.2 x 75.2 x 8.1 mm (6.27 x 2.96 x 0.32 in), It has front/back glass (Gorilla Glass 5), It comes with Hybrid Dual SIM (Nano-SIM, dual stand-by), It offers a premium & impressive design.**

**Xiaomi Redmi Note 7 Pro has a loudspeaker, It comes with 3.5mm jack, It contains active noise cancellation with dedicated mic, It has Comms WLAN such as Wi-Fi 802.11 a/b/g/n/ac, dual-band, Wi-Fi Direct, hotspot, It presents Bluetooth 5.0, A2DP, LE and it offers high build quality.**

**Xiaomi Redmi Note 7 Pro has GPS, with A-GPS, GLONASS, BDS, It supports Infraredport, It has FM radio, recording, It offers USB 2.0, Type-C 1.0 reversible connector, It comes with a rich number of sensors such as fingerprint (rear-mounted), accelerometer, gyro, ambient light sensor, proximity & compass.**

**Xiaomi Redmi Note 7 Pro comes with a non-removable Li-Po 4000 mAh battery that lasts for a long time, It presents fast battery charging 18W (Quick Charge 4), It has misc colors such as Nebula Red, Neptune Blue, Space Black and its price is About 200 EUR.**

**Xiaomi Redmi Note 7 Pro comes with premium design, It contains a long battery life, It offers smooth performance, It supports 4G in India (Band 40), It looks very premium in the hands, It offers a high pixel density, It has a high resolution that makes the display very clear & bright.**

**Xiaomi Redmi Note 7 Pro offers a high-end processor & graphics processor, It has excellent & up-to-date software, It supports superb cameras with many features, It has a big & vibrant screen, It provides you with better viewing angles & lower power consumption, It offers nearly every connectivity like Wi-Fi, Bluetooth, GPS, USB, 3G & 4G.**

**10.2 Xiaomi Redmi Note 7 Pro disadvantages**

**Xiaomi Redmi Note 7 Pro comes with a bit heavy weight of 186 g (6.56 oz), It comes with a non-removable battery, It heats up quickly, It does not have an NFC feature, it does not offer a water & dust resistant, It does not have wireless charging, It does not have Barometer or Temperature sensor**

**Pros**

* Excellent performance
* Excellent rear camera
* Elegant glass finish
* USB Type-C and QuickCharge 4.0 support
* Decent battery backup
* Aggressive price

**Cons**

* Ads in the UI (can be mostly turned off)
* Hybrid card slot
* No HD streaming on Netflix and Prime
* Fast charger not bundled in the box
* Gets hot with extended gaming
* That camera hump isn’t easy to even

**11. Compare Nokia 6100 vs Redmi Note 7 Pro**

### SUMMARY

CRITIC RATING

* N/A
* N/A

USER RATING

* N/A
* N/A

### SPECIAL FEATURES

JAVA

* No
* -

BROWSER

* Yes
* -

### GENERAL

SIM SLOTS

* Single SIM, GSM
* Dual SIM, GSM+GSM

MODEL

* 6100
* Mi 4C

LAUNCH DATE

* September 1, 2002
* -

BRAND

* Nokia
* Xiaomi

NETWORK

* 2G: Available
* 4G: Available (supports Indian bands) 3G: Available, 2G: Available

### MULTIMEDIA

MUSIC

* Yes Music Formats: No
* -

### DESIGN

THICKNESS

* 13.50 mm
* -

WIDTH

* 44.00 mm
* -

WEIGHT

* 76 grams
* 132 grams

HEIGHT

* 102.00 mm
* -

### DISPLAY

SCREEN RESOLUTION

* 128.00 x 128 pixels
* Full HD (1080 x 1920 pixels)

### STORAGE

EXPANDABLE MEMORY

* Yes
* No

### CAMERA

MAIN CAMERA

* No
* Yes, 13 MP, Auto focus

### BATTERY

STANDBY TIME

* Up to 320(2G)
* -

TALKTIME

* Up to 6(2G)
* -

### NETWORK CONNECTIVITY

BLUETOOTH

* No
* Yes, v4.1

NETWORK SUPPORT

* 2G
* 4G (supports Indian bands), 3G, 2G

SIM 1

* GPRS: Class 4, 24 - 36 kbps
* 4G Bands:TD-LTE 2600(band 38) / 2300(band 40) / 2500(band 41) / 1900(band 39) FD-LTE 2100(band 1) / 1800(band 3) / 2600(band 7) 3G Bands: UMTS 1900 / 2100 / 850 / 900 MHz 2G Bands: GSM 1800 / 1900 / 850 / 900 MHz 4G Speed: 50 Mbit/ s ? 150 Mbit/ s ? (LTE category 4) GPRS:AvailableEDGE:Available

### MORE DETAILS

PRICE

* ₹ 2,999
* ₹ 13,990

**End**

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**Nokia6100**



**INTRODUCTION**

The **Nokia 6100** is a popular mid-range [Nokia](https://en.wikipedia.org/wiki/Nokia) [mobile phone](https://en.wikipedia.org/wiki/Mobile_phone) that was available from 2002 to 2005. It was announced on 4 September 2002 (together with [Nokia 7250](https://en.wikipedia.org/wiki/Nokia_7250))

The Nokia 6100 was Nokia’s lightest phone with a full 12-key keypad at the time. Combined with its battery, it weighs only 76 grams (2.68 ounces) and measures 102 x 44 x 13.5 mm. Its smaller size compared with other contemporary phones might make it difficult for the elderly, or people with large fingers, to use its keypad. The phone supports Xpress-On covers, and is packaged along with any of 4 colors. Its feature set is very similar to the [Nokia 7210](https://en.wikipedia.org/wiki/Nokia_7210), although with a more conservative design.

The Nokia 6100 has a display with a resolution of 128 x 128 pixels, featuring 12-bit color (allowing for 4096 possible colors). Its features include [Internet](https://en.wikipedia.org/wiki/Internet) connectivity via [GPRS](https://en.wikipedia.org/wiki/GPRS), an [infrared port](https://en.wikipedia.org/wiki/Infrared_port), inbuilt calendar and polyphonic [ring tones](https://en.wikipedia.org/wiki/Ringtone). It does not have a [camera](https://en.wikipedia.org/wiki/Digital_camera). It could be considered the true successor of the [Nokia 8210](https://en.wikipedia.org/wiki/Nokia_8210) and Nokia 8250 in terms of design functionality and its small flat size.

The LCD screen comes in two main versions which are very similar. One version of the LCD is controlled by an [EPSON](https://en.wikipedia.org/wiki/EPSON) S1D15G00 driver chip, whilst the other version uses a [Philips](https://en.wikipedia.org/wiki/Philips) PCF8833 instead. There are also clones of these drivers. Early releases had a slightly blurry, yellower and duller screen compared with the Nokia 7210 and [6610](https://en.wikipedia.org/wiki/Nokia_6610) of the same period, but later screens improved this shortcoming.

Both driver chips allow the display to be used with 8-bit (256 colors) or 12-bit (4096 colors) RGB. Only the Philips version provides, on a low-level, the ability to use 16-bit RGB. This is achieved through dithering. 16-bit RGB gives 65536 different colors, sixteen times that available in the Nokia 12-bit RGB color mode.

\

* FULL SPECIFICATION
* **Phone Features**
  1. Tri-band world phone – works in three networks on five continents
  2. Downloadable personal applications via Java™ technology
  3. MMS (Multimedia Messaging)
  4. GPRS (General Packet Radio Service)
  5. HSCSD (High Speed Data)
  6. Wallet
  7. WIM (Wireless Identity Module)
  8. WAP 1.2.1 Browser (via GRPS or CSD)
  9. Hands free speaker
  10. Customizable and timed profiles
  11. Polyphonic ringing tones
  12. Wallpaper: full screen color image
  13. Screen saver: digital clock
  14. Clock, alarm clock
  15. Calculator, currency converter
  16. Stopwatch, countdown timer
  17. Connectivity options: IR and cable
  18. Hands free speaker Customizable and timed profiles
  19. Hands free Speaker: With adjustable volume
  20. User Profiles: Timed and user configurable

* **SIZE**

1. Weight: 76 g (battery included)
2. Dimensions: 102 x 44 x 13.5, 60 cc

* **DISPLAY**

1. High-resolution, passive Matrix Color Display
2. Supports 4096 colors within 128×128 pixels
3. Up to 8 lines (Latin) / 6 lines (Chinese) in message viewing
4. Adjustable display brightness control

* **MEMORY FUNCTIONS**

1. Phone book (up to 300 entries)
2. SMSs (up to 150 text messages or 50 picture/concatenated messages)
3. Fixed ringing tones (11 preset, not removable)
4. Calendar notes (up to 250 entries)
5. To-do list (up to 30 entries)

The following features share a memory pool of 669 KB:

1. MMS messages (max size 45 KB per MMS message)
2. Ringing tones in Gallery (20 preset, all removable)
3. Images (10 preset, up to 35 average size 10 KB images)
4. Java&153; applications (3 preset, up to 6 max size 64 KB per application)

* **MESSAGING**

1. Text messaging: concatenated SMS, send and receive up to 3 messages, (459)160+146+153 characters, in Unicode 70+63+63 per message
2. Predictive text input: support for all major European languages
3. Templates: quick and easy sending of pre-defined messages
4. Picture messaging: send pictures with text to other compatible phones. 10 predefined pictures in the phone, 5 empty for downloads, all replaceable.
5. Multimedia messaging: receive messages containing a text, a audio file and a image, which can be saved as wallpaper and ringing tone; send and forward messages containing images and text to other compatible phones.
6. Mobile Chat: based on standard SMS. All previous written messages from both persons are visible on screen. Chat messages are not saved on the SIM card.

* **RINGING TONES**

1. 21 polyphonic and 10 monophonic tones preinstalled

* **PREINSTALLED JAVA™ APPLICATIONS**

1. Converter II (Currency, area, length, mass, temperature etc. conversions)
2. World Clock II
3. Games: Puzzle Chess
4. All applications user removable

* **CALL MANAGEMENT**

1. Speed dialing: for up to 9 names (key 1 is always for voice mail)
2. Last numbers redial from dialed calls list (key brings out the dialed calls list)
3. Automatic redial (max 10 attempts)
4. Automatic answer (works with headset or car kit only)
5. Emergency calls to 112 without SIM-card and with key locked phone
6. Call waiting, call hold, call divert, call timer
7. Automatic and manual network selection
8. Closed User Group
9. Fixed Dialing Number, allows calls only to predefined numbers
10. Voice dialing is not supported.

* **TRI-BAND OPERATION**

1. EGSM 900, GSM 1800 and GSM 1900 networks in Europe, Africa, Asia, North and South America.
2. Automatic switching between the bands.

* **POP-PORT**

1. Stereo sound is not supported

**PROCESSOR AND ARCHITECHTURE**

An ARM processor is one of a family of [CPUs](https://whatis.techtarget.com/definition/processor) based on the [RISC](https://search400.techtarget.com/definition/RISC) (reduced instruction set computer) architecture developed by Advanced RISC Machines (ARM).

ARM makes 32-bit and [64-bit](https://searchdatacenter.techtarget.com/definition/64-bit-processor) RISC [multi-core processors](https://searchdatacenter.techtarget.com/definition/multi-core-processor). RISC [processors](https://whatis.techtarget.com/definition/microprocessor-logic-chip) are designed to perform a smaller number of types of computer [instructions](https://whatis.techtarget.com/definition/instruction) so that they can operate at a higher speed, performing more millions of instructions per second ([MIPS](https://searchitoperations.techtarget.com/definition/MIPS-million-instructions-per-second)).  By stripping out unneeded instructions and optimizing pathways, RISC processors provide outstanding performance at a fraction of the power demand of [CISC](https://whatis.techtarget.com/definition/CISC-complex-instruction-set-computer-or-computing) (complex instruction set computing) devices.

ARM processor features include:

* Load/store architecture.
* An [orthogonal](https://searchstorage.techtarget.com/definition/orthogonal) instruction set.
* Mostly single-cycle execution.
* Enhanced power-saving design.
* 64 and 32-bit execution states for scalable high performance.
* [Hardware virtualization](https://searchservervirtualization.techtarget.com/definition/hardware-virtualization) support.

The simplified design of ARM processors enables more efficient multi-core processing and easier coding for developers. While they don't have the same raw compute [throughput](https://searchnetworking.techtarget.com/definition/throughput) as the products of [x86](https://searchwindowsserver.techtarget.com/definition/x86) market leader Intel, ARM processors sometimes exceed the performance of Intel processors for applications that exist on both architectures.

The head-to-head competition between the vendors is increasing as ARM is finding its way into full size notebooks.  Microsoft, for example, offers ARM-based versions of Surface computers. The cleaner code base of [WindowsRT](https://whatis.techtarget.com/definition/Windows-RT) versus x86 versions may be also partially responsible -- Windows RT is more streamlined because it doesn’t have to support a number of legacy hardware.

ARM is also moving into the server market,  a move that represents a large change in direction and a hedging of bets on performance-per-watt over raw compute power. AMD offers 8-core versions of ARM processors for its Opteron series of processors. [ARM servers](https://searchdatacenter.techtarget.com/definition/advanced-RISC-machine-ARM) represent an important shift in server-based computing. A traditional x86-class server with 12, 16, 24 or more cores increases performance by [scaling](https://searchdatacenter.techtarget.com/definition/scalability) up the speed and sophistication of each processor, using brute force speed and power to handle demanding computing workloads.

In comparison, an ARM server uses perhaps hundreds of smaller, less sophisticated, low-power processors that share processing tasks among that large number instead of just a few higher-capacity processors. This approach is sometimes referred to as “scaling out,” in contrast with the “scaling up” of x86-based servers.

The ARM architecture was originally developed by Acorn Computers in the 1980s.

This NOKIA 6100 mobile used ARM for processor to perform their operations. This mobile has 1 number of core processor and it uses 0.70mb built in memory space.

**INSTRUCTION SET**

An **instruction set architecture** (**ISA**) is an abstract model of a [computer](https://en.wikipedia.org/wiki/Computer). It is also referred to as **architecture** or **computer architecture**. A realization of an ISA is called an *implementation*. An ISA permits multiple implementations that may vary in [performance](https://en.wikipedia.org/wiki/Computer_performance), physical size, and monetary cost (among other things); because the ISA serves as the [interface](https://en.wikipedia.org/wiki/Interface_(computing)) between [software](https://en.wikipedia.org/wiki/Software) and [hardware](https://en.wikipedia.org/wiki/Computer_hardware). Software that has been written for an ISA can run on different implementations of the same ISA. This has enabled [binarycompatibility](https://en.wikipedia.org/wiki/Binary_compatibility) between different generations of computers to be easily achieved, and the development of computer families. Both of these developments have helped to lower the cost of computers and to increase their applicability. For these reasons, the ISA is one of the most important abstractions in [computing](https://en.wikipedia.org/wiki/Computing) today.

An ISA defines everything a [machinelanguage](https://en.wikipedia.org/wiki/Machine_language) [programmer](https://en.wikipedia.org/wiki/Programmer) needs to know in order to program a computer. What an ISA defines differs between ISAs; in general, ISAs define the supported [datatypes](https://en.wikipedia.org/wiki/Data_type), what state there is (such as the [mainmemory](https://en.wikipedia.org/wiki/Main_memory) and [registers](https://en.wikipedia.org/wiki/Processor_register)) and their semantics (such as the [memoryconsistency](https://en.wikipedia.org/wiki/Memory_consistency) and [addressingmodes](https://en.wikipedia.org/wiki/Addressing_mode)), the instruction set (the set of [machineinstructions](https://en.wikipedia.org/wiki/Machine_instruction) that comprises a computer's machine language), and the [input/output](https://en.wikipedia.org/wiki/Input/output) model.

* **CLASSIFICATION OF ISAs**

An ISA may be classified in a number of different ways. A common classification is by architectural *complexity*. A [complex instruction set computer](https://en.wikipedia.org/wiki/Complex_instruction_set_computer) (CISC) has many specialized instructions, some of which may only be rarely used in practical programs. A [reduced instruction set computer](https://en.wikipedia.org/wiki/Reduced_instruction_set_computer) (RISC) simplifies the processor by efficiently implementing only the instructions that are frequently used in programs, while the less common operations are implemented as subroutines, having their resulting additional processor execution time offset by infrequent use.[[2]](https://en.wikipedia.org/wiki/Instruction_set_architecture#cite_note-2)

Other types include [very long instruction word](https://en.wikipedia.org/wiki/Very_long_instruction_word) (VLIW) architectures, and the closely related *long instruction word* (LIW) and [*explicitly parallel instruction computing*](https://en.wikipedia.org/wiki/Explicitly_parallel_instruction_computing) (EPIC) architectures. These architectures seek to exploit [instruction-level parallelism](https://en.wikipedia.org/wiki/Instruction-level_parallelism) with less hardware than RISC and CISC by making the [compiler](https://en.wikipedia.org/wiki/Compiler) responsible for instruction issue and scheduling.

Architectures with even less complexity have been studied, such as the [minimal instruction set computer](https://en.wikipedia.org/wiki/Minimal_instruction_set_computer) (MISC) and [one instruction set computer](https://en.wikipedia.org/wiki/One_instruction_set_computer) (OISC). These are theoretically important types, but have not been commercialized.

* **INSTRUCTIONS**

[Machine language](https://en.wikipedia.org/wiki/Machine_code) is built up from discrete *statements* or *instructions*. On the processing architecture, a given instruction may specify:

* particular [registers](https://en.wikipedia.org/wiki/Processor_register) (for arithmetic, addressing, or control functions)
* particular memory locations (or offsets to them)
* particular [addressing modes](https://en.wikipedia.org/wiki/Addressing_mode) (used to interpret the operands)

More complex operations are built up by combining these simple instructions, which are executed sequentially, or as otherwise directed by [control flow](https://en.wikipedia.org/wiki/Control_flow) instructions.

### INSTRUCTION TYPE

Examples of operations common to many instruction sets include:

* **DATA HANDLING AND MEMORY OPERATIONS**
* Set a [register](https://en.wikipedia.org/wiki/Processor_register) to a fixed constant value.
* Copy data from a memory location to a register, or vice versa (a machine instruction is often called move; however, the term is misleading). Used to store the contents of a register, the result of a computationor to retrieve stored data to perform a computation on it later. Often called [load and store](https://en.wikipedia.org/wiki/Load_and_store) operations.
* Read and write data from hardware devices.

#### [ARITHMETIC AND LOGIC](https://en.wikipedia.org/wiki/Arithmetic_logic_unit) OPERATIONS

* Add, subtract, multiply, or divide the values of two registers, placing the result in a register, possibly setting one or more [condition codes](https://en.wikipedia.org/wiki/Flag_(computing)) in a [status register](https://en.wikipedia.org/wiki/Status_register).
* Increment, decrement in some ISAs, saving operand fetch in trivial cases.
* Perform [bitwise operations](https://en.wikipedia.org/wiki/Bitwise_operation), e.g., taking the [conjunction](https://en.wikipedia.org/wiki/Logical_conjunction) and [disjunction](https://en.wikipedia.org/wiki/Logical_disjunction) of corresponding bits in a pair of registers, taking the [negation](https://en.wikipedia.org/wiki/Logical_negation) of each bit in a register.
* Compare two values in registers (for example, to see if one is less, or if they are equal).
* Floating-point instructions for arithmetic on floating-point numbers.

#### [CONTROL FLOW](https://en.wikipedia.org/wiki/Control_flow) OPERATIONS

* [Branch](https://en.wikipedia.org/wiki/Branch_(computer_science)) to another location in the program and execute instructions there.
* [Conditionally branch](https://en.wikipedia.org/wiki/Branch_predication) to another location if a certain condition holds.
* [Indirectly branch](https://en.wikipedia.org/wiki/Indirect_branch) to another location.
* [Call](https://en.wikipedia.org/wiki/Subroutine) another block of code, while saving the location of the next instruction as a point to return to.

#### [COPROCESSOR](https://en.wikipedia.org/wiki/Coprocessor) INSTRUCTIONS

* Load/store data to and from a coprocessor or exchanging with CPU registers.
* Perform coprocessor operations.

### COMPLEX INSTRUCTIONS

Processors may include "complex" instructions in their instruction set. A single "complex" instruction does something that may take many instructions on other computers such instructions are [typified](https://en.wikipedia.org/wiki/Typified) by instructions that take multiple steps, control multiple functional units, or otherwise appear on a larger scale than the bulk of simple instructions implemented by the given processor. Some examples of "complex" instructions include:

* Transferring multiple registers to or from memory (especially the [stack](https://en.wikipedia.org/wiki/Call_stack)) at once
* Moving large blocks of memory (e.g. [string copy](https://en.wikipedia.org/wiki/String_copy) or [DMA transfer](https://en.wikipedia.org/wiki/DMA_transfer))
* Complicated integer and floating-point arithmetic (e.g. [square root](https://en.wikipedia.org/wiki/Square_root), or [transcendental functions](https://en.wikipedia.org/wiki/Transcendental_function) such as [logarithm](https://en.wikipedia.org/wiki/Logarithm), [sine](https://en.wikipedia.org/wiki/Sine), [cosine](https://en.wikipedia.org/wiki/Cosine), etc.)
* [SIMD](https://en.wikipedia.org/wiki/SIMD) instructions, a single instruction performing an operation on many homogeneous values in parallel, possibly in dedicated [SIMD registers](https://en.wikipedia.org/wiki/SIMD_register)
* Performing an atomic [test-and-set](https://en.wikipedia.org/wiki/Test-and-set) instruction or other [read-modify-write](https://en.wikipedia.org/wiki/Read-modify-write) [atomic instruction](https://en.wikipedia.org/wiki/Atomic_instruction)
* Instructions that perform [ALU](https://en.wikipedia.org/wiki/Arithmetic_logic_unit) operations with an operand from memory rather than a register.

Complex instructions are more common in CISC instruction sets than in RISC instruction sets, but RISC instruction sets may include them as well. RISC instruction sets generally do not include ALU operations with memory operands, or instructions to move large blocks of memory, but most RISC instruction sets include [SIMD](https://en.wikipedia.org/wiki/SIMD) or [vector](https://en.wikipedia.org/wiki/Vector_processing) instructions that perform the same arithmetic operation on multiple pieces of data at the same time. SIMD instructions have the ability of manipulating large vectors and matrices in minimal time. SIMD instructions allow easy [parallelization](https://en.wikipedia.org/wiki/Parallelization) of algorithms commonly involved in sound, image, and video processing. Various SIMD implementations have been brought to market under trade names such as [MMX](https://en.wikipedia.org/wiki/MMX_(instruction_set)), [3DNow!](https://en.wikipedia.org/wiki/3DNow!).

* **INSTRUCTION ENCODING**

On traditional architectures, an instruction includes an [opcode](https://en.wikipedia.org/wiki/Opcode) that specifies the operation to perform, such as *add contents of memory to register*—and zero or more [operand](https://en.wikipedia.org/wiki/Operand) specifiers, which may specify [registers](https://en.wikipedia.org/wiki/Processor_register), memory locations, or literal data. The operand specifiers may have [addressing modes](https://en.wikipedia.org/wiki/Addressing_mode) determining their meaning or may be in fixed fields. In [very long instruction word](https://en.wikipedia.org/wiki/Very_long_instruction_word) (VLIW) architectures, which include many [microcode](https://en.wikipedia.org/wiki/Microcode) architectures, multiple simultaneous opcodes and operands are specified in a single instruction.

Some exotic instruction sets do not have an opcode field, such as [transport triggered architectures](https://en.wikipedia.org/wiki/Transport_triggered_architecture) (TTA), only operand(s).

The [Forth virtual machine](https://en.wikipedia.org/wiki/Forth_virtual_machine) and other "[0-operand](https://en.wikipedia.org/wiki/0-operand_instruction_set)" instruction sets lack any operand specifier fields, such as some [stack machines](https://en.wikipedia.org/wiki/Stack_machine) including NOSC.[[3]](https://en.wikipedia.org/wiki/Instruction_set_architecture#cite_note-3)[[*better source needed*](https://en.wikipedia.org/wiki/Wikipedia:NOTRS)]

Conditional instructions often have a predicate field—a few bits that encode the specific condition to cause the operation to be performed rather than not performed. For example, a conditional branch instruction will be executed, and the branch taken, if the condition is true, so that execution proceeds to a different part of the program, and not executed, and the branch not taken, if the condition is false, so that execution continues sequentially. Some instruction sets also have conditional moves, so that the move will be executed, and the data stored in the target location, if the condition is true, and not executed, and the target location not modified, if the condition is false. Similarly, IBM [z/Architecture](https://en.wikipedia.org/wiki/Z/Architecture) has a conditional store instruction. A few instruction sets include a predicate field in every instruction; this is called [branch predication](https://en.wikipedia.org/wiki/Branch_predication).

#### NUMBER OF OPERANDS

Instruction sets may be categorized by the maximum number of operands explicitly specified in instructions.

(In the examples that follow, A, B, and C are (direct or calculated) addresses referring to memory cells, while reg1 and so on refer to machine registers.)

C = A+B

* 0-operand (zero-address machines), so called [stack machines](https://en.wikipedia.org/wiki/Stack_machine): All arithmetic operations take place using the top one or two positions on the stack: push a, push b, add, pop c.
* C = A+B needs four instructions. For stack machines, the terms "0-operand" and "zero-address" apply to arithmetic instructions, but not to all instructions, as 1-operand push and pop instructions are used to access memory.

1. 1-operand (one-address machines), so called [accumulator machines](https://en.wikipedia.org/wiki/Accumulator_machine), include early computers and many small [microcontrollers](https://en.wikipedia.org/wiki/Microcontroller): most instructions specify a single right operand (that is, constant, a register, or a memory location), with the implicit [accumulator](https://en.wikipedia.org/wiki/Accumulator_(computing)) as the left operand (and the destination if there is one): load a, add b, store c.

* C = A+B needs three instructions.

1. 2-operand — many CISC and RISC machines fall under this category:

* CISC — move A to C; then add B to C.
* C = A+B needs two instructions. This effectively 'stores' the result without an explicit store instruction.
* CISC — Often machines are [limited to one memory operand](https://web.archive.org/web/20131105155703/http:/cs.smith.edu/~thiebaut/ArtOfAssembly/CH04/CH04-3.html#HEADING3-79) per instruction: load a,reg1; add b,reg1; store reg1,c; This requires a load/store pair for any memory movement regardless of whether the add result is an augmentation stored to a different place, as in C = A+B, or the same memory location: A = A+B.
* C = A+B needs three instructions.
* RISC — Requiring explicit memory loads, the instructions would be: load a,reg1; load b,reg2; add reg1,reg2; store reg2,c.
  + - C = A+B needs four instructions.

1. 3-operand, allowing better reuse of data:[[4]](https://en.wikipedia.org/wiki/Instruction_set_architecture#cite_note-Cocke-4)

* CISC — It becomes either a single instruction: add a,b,c
  + - C = A+B needs one instruction.
* CISC — Or, on machines limited to two memory operands per instruction, move a,reg1; add reg1,b,c;
* C = A+B needs two instructions.
* RISC — arithmetic instructions use registers only, so explicit 2-operand load/store instructions are needed: load a,reg1; load b,reg2; add reg1+reg2->reg3; store reg3,c;
* C = A+B needs four instructions.
* Unlike 2-operand or 1-operand, this leaves all three values a, b, and c in registers available for further reuse.[[4]](https://en.wikipedia.org/wiki/Instruction_set_architecture#cite_note-Cocke-4)
* More operands—some CISC machines permit a variety of addressing modes that allow more than 3 operands (registers or memory accesses), such as the [VAX](https://en.wikipedia.org/wiki/VAX) "POLY" polynomial evaluation instruction.

Due to the large number of bits needed to encode the three registers of a 3-operand instruction, RISC architectures that have 16-bit instructions are invariably 2-operand designs, such as the Atmel AVR, [TI MSP430](https://en.wikipedia.org/wiki/TI_MSP430), and some versions of [ARM Thumb](https://en.wikipedia.org/wiki/ARM_Thumb). RISC architectures that have 32-bit instructions are usually 3-operand designs, such as the [ARM](https://en.wikipedia.org/wiki/ARM_architecture), [AVR32](https://en.wikipedia.org/wiki/AVR32), [MIPS](https://en.wikipedia.org/wiki/MIPS_architecture), [Power ISA](https://en.wikipedia.org/wiki/Power_ISA), and [SPARC](https://en.wikipedia.org/wiki/SPARC) architectures.

Each instruction specifies some number of operands (registers, memory locations, or immediate values) explicitly. Some instructions give one or both operands implicitly, such as by being stored on top of the [stack](https://en.wikipedia.org/wiki/Stack_(data_structure)) or in an implicit register. If some of the operands are given implicitly, fewer operands need be specified in the instruction. When a "destination operand" explicitly specifies the destination, an additional operand must be supplied. Consequently, the number of operands encoded in an instruction may differ from the mathematically necessary number of arguments for a logical or arithmetic operation. Operands are either encoded in the "Opcode" representation of the instruction, or else are given as values or addresses following the instruction.

* **INSTRUCTION SET IMPLEMENTATION**

Any given instruction set can be implemented in a variety of ways. All ways of implementing a particular instruction set provide the same [programming model](https://en.wikipedia.org/wiki/Programming_model), and all implementations of that instruction set are able to run the same executable. The various ways of implementing an instruction set give different tradeoffs between cost, performance, power consumption, size, etc.

When designing the [microarchitecture](https://en.wikipedia.org/wiki/Microarchitecture) of a processor, engineers use blocks of "hard-wired" electronic circuitry (often designed separately) such as adders, multiplexers, counter, registers, ALUs, etc. Some kind of [register transfer language](https://en.wikipedia.org/wiki/Register_transfer_language) is then often used to describe the decoding and sequencing of each instruction of an ISA using this physical microarchitecture. There are two basic ways to build a [control unit](https://en.wikipedia.org/wiki/Control_unit) to implement this description (although many designs use middle ways or compromises):

Some computer designs "hardwire" the complete instruction set decoding and sequencing (just like the rest of the microarchitecture).

Other designs employ [microcode](https://en.wikipedia.org/wiki/Microcode) routines or tables (or both) to do this—typically as on-chip [ROMs](https://en.wikipedia.org/wiki/Read-only_memory) or [PLAs](https://en.wikipedia.org/wiki/Programmable_logic_array) or both (although separate RAMs and [ROMs](https://en.wikipedia.org/wiki/Read-only_memory#Historical_examples) have been used historically). The [Western Digital](https://en.wikipedia.org/wiki/Western_Digital) [MCP-1600](https://en.wikipedia.org/wiki/MCP-1600) is an older example, using a dedicated, separate ROM for microcode.

Some designs use a combination of hardwired design and microcode for the control unit.

Some CPU designs use a [writable control store](https://en.wikipedia.org/wiki/Writable_control_store)—they compile the instruction set to a writable [RAM](https://en.wikipedia.org/wiki/RAM) or [flash](https://en.wikipedia.org/wiki/Flash_memory) inside the CPU (such as the [Recursive](https://en.wikipedia.org/wiki/Rekursiv) processor and the [Imsys](https://en.wikipedia.org/w/index.php?title=Imsys&action=edit&redlink=1) Chip),[[10]](https://en.wikipedia.org/wiki/Instruction_set_architecture#cite_note-10) or an FPGA ([reconfigurable computing](https://en.wikipedia.org/wiki/Reconfigurable_computing)).

An ISA can also be [emulated](https://en.wikipedia.org/wiki/Emulator) in software by an [interpreter](https://en.wikipedia.org/wiki/Interpreter_(computing)). Naturally, due to the interpretation overhead, this is slower than directly running programs on the emulated hardware, unless the hardware running the emulator is an order of magnitude faster. Today, it is common practice for vendors of new ISAs or microarchitectures to make software emulators available to software developers before the hardware implementation is ready.

Often the details of the implementation have a strong influence on the particular instructions selected for the instruction set. For example, many implementations of the [instruction pipeline](https://en.wikipedia.org/wiki/Instruction_pipeline) only allow a single memory load or memory store per instruction, leading to a [load-store architecture](https://en.wikipedia.org/wiki/Load-store_architecture) (RISC). For another example, some early ways of implementing the [instruction pipeline](https://en.wikipedia.org/wiki/Instruction_pipeline) led to a [delay slot](https://en.wikipedia.org/wiki/Delay_slot).

The demands of high-speed digital signal processing have pushed in the opposite direction—forcing instructions to be implemented in a particular way. For example, to perform digital filters fast enough, the MAC instruction in a typical [digital signal processor](https://en.wikipedia.org/wiki/Digital_signal_processor) (DSP) must use a kind of [Harvard architecture](https://en.wikipedia.org/wiki/Harvard_architecture) that can fetch an instruction and two data words simultaneously, and it requires a single-cycle [multiply–accumulate](https://en.wikipedia.org/wiki/Multiply%E2%80%93accumulate) [multiplier](https://en.wikipedia.org/wiki/Binary_multiplier).

**MEMORY ORGANIZATION**

**Memory** is the faculty of the [brain](https://en.wikipedia.org/wiki/Brain) by which [data](https://en.wikipedia.org/wiki/Data) or [information](https://en.wikipedia.org/wiki/Information) is encoded, stored, and retrieved when needed. It is the retention of information over time for the purpose of influencing future action. If [past events](https://en.wikipedia.org/wiki/Foresight_(psychology)) could not be remembered, it would be impossible for language, relationships, or [personal identity](https://en.wikipedia.org/wiki/Personal_identity) to develop. Memory loss is usually described as [forgetfulness](https://en.wikipedia.org/wiki/Forgetting) or [amnesia](https://en.wikipedia.org/wiki/Amnesia).

Memory is often understood as an [informational processing](https://en.wikipedia.org/wiki/Information_processing) system with explicit and implicit functioning that is made up of a [sensory processor](https://en.wikipedia.org/wiki/Sensory_processor), [short-term](https://en.wikipedia.org/wiki/Short-term_memory) (or [working](https://en.wikipedia.org/wiki/Working_memory)) memory, and [long-term memory](https://en.wikipedia.org/wiki/Long-term_memory).[[9]](https://en.wikipedia.org/wiki/Memory#cite_note-Baddeley_2007-9) This can be related to the [neuron](https://en.wikipedia.org/wiki/Neuron). The sensory processor allows information from the outside world to be sensed in the form of chemical and physical stimuli and attended to various levels of focus and intent. Working memory serves as an encoding and retrieval processor. Information in the form of stimuli is encoded in accordance with explicit or implicit functions by the working memory processor. The working memory also retrieves information from previously stored material. Finally, the function of long-term memory is to store data through various categorical models or systems.

[Declarative, or explicit, memory](https://en.wikipedia.org/wiki/Explicit_memory) is the conscious storage and recollection of data.Under declarative memory resides [semantic](https://en.wikipedia.org/wiki/Semantic_memory) and [episodic memory](https://en.wikipedia.org/wiki/Episodic_memory). Semantic memory refers to memory that is encoded with specific meaningwhile episodic memory refers to information that is encoded along a spatial and temporal plane.Declarative memory is usually the primary process thought of when referencing memory.[Non-declarative, or implicit, memory](https://en.wikipedia.org/wiki/Implicit_memory) is the unconscious storage and recollection of information.An example of a non-declarative process would be the unconscious learning or retrieval of information by way of [procedural memory](https://en.wikipedia.org/wiki/Procedural_memory), or a priming phenomenon.[Priming](https://en.wikipedia.org/wiki/Priming_(psychology)) is the process of [subliminally](https://en.wikipedia.org/wiki/Subliminal_stimuli) arousing specific responses from memory and shows that not all memory is consciously activated.whereas procedural memory is the slow and gradual learning of skills that often occurs without conscious attention to learning.

Memory is not a perfect processor, and is affected by many factors. The ways by which information is encoded, stored, and retrieved can all be corrupted? The amount of attention given new stimuli can diminish the amount of information that becomes encoded for storage.Also, the storage process can become corrupted by physical damage to areas of the brain that are associated with memory storage, such as the hippocampus.Finally, the retrieval of information from long-term memory can be disrupted because of decay within long-term memory.Normal functioning, decay over time, and brain damage all affect the accuracy and capacity of the memory

**Shared Memory is used by this NOKIA 6100 Mobile**

Thefollowingfeaturesinyourphoneusesharedmemory:Phonebook, textandmultimediamessages,imagesandringingtonesingallery, calendarandto-donotes,andJavagamesandapplications.Usinganyof thesefeaturesleaveslessmemoryforotherfeatures.Thisisespecially truewithheavyuseofanyofthefeatures.Forexample,savingmany imagesmaytakeallofthesharedmemoryandyourphonemaydisplay thatthememoryisfull.Inthiscase,deletesomeoftheinformationor entries reserving the sharedmemory.

Thefollowingfunctionsusesharedmemorythatisdependentonthe dataquantityperitemandsharedmemoryavailableatatimeinthe Nokia6100:

Phone book (up to 300entries)

SMS(upto150textmessagesor50picture/concatenatedmessages)

Calendarnotes(upto250entries)

To-do list (up to 30entries)

Fixedringtones(11presets,notremovable)

The following features share a memory pool of 725kB:

MMSmessages(maxsizeof45KBperMMSmessage)

RingtonesinGallery(20preset,allremovable)

ImagesinGallery(10preset,allremovable)

Javaapplications(3preset,maxdownloadsize64kBperapplication) Thefollowingfunctionsusestaticmemory:

WAP cache (up to 20entries)

WAPbookmarks(upto30entries)

WAPsecuritycacheandcertificates(upto20entries)

**CONTROL UNIT**

Definition – What does Control Unit (CU*)* mean?

A control unit (CU) handles all processor control signals. It directs all input and output flow, fetches code for instructions from micro programs and directs other units and models by providing control and timing signals. A CU component is considered the processor brain because it issues orders to just about everything and ensures correct instruction execution.

A CU takes its input from the instruction and status registers. Its rules of operation, or micro program, are encoded in a programmable logic array (PLA), random logic or read-only memory.  
  
CU functions are as follows:

* Controls sequential instruction execution
* Interprets instructions
* Guides data flow through different mobile areas
* Regulates and controls processor timing
* Sends and receives control signals from other mobile devices
* Handles multiple tasks, such as fetching, decoding, execution handling and storing results

Control Unitis designed in two ways:

* Hardwired control: Design is based on a fixed architecture. The CU is made up of flip-flops, logic gates, digital circuits and encoder and decoder circuits that are wired in a specific and fixed way. When instruction set changes are required, wiring and circuit changes must be made. This is preferred in a reduced instruction set computing (RISC) architecture, which only has a small number of instructions.
* Micro program control: Micro programs are stored in a special control memory and are based on flowcharts. They are replaceable and ideal because of their simplicity.

**I/O MECHANISMS**

In mobile computing, **input/output** or **I/O**is the communication between an [information processing system](https://en.wikipedia.org/wiki/Information_processing_system), such as a mobile and the outside world, possibly a human or another [information processing system](https://en.wikipedia.org/wiki/Information_processor). [Inputs](https://en.wikipedia.org/wiki/Information) are the signals or data received by the system and outputs are the signals or [data](https://en.wikipedia.org/wiki/Data_(computing)) sent from it. The term can also be used as part of an action; to "perform I/O" is to perform an [input or output operation](https://en.wikipedia.org/wiki/I/O_scheduling).

**I/O devices** are the pieces of [hardware](https://en.wikipedia.org/wiki/Hardware_(computing)) used by a human (or other system) to communicate with a mobile. For instance, a keypad or keyboard isan [input device](https://en.wikipedia.org/wiki/Input_device) for a mobile, while display is output devices. Devices for communication between mobiles, such as internet connection typically perform both input and output operations.

The designation of a device as either input or output depends on perspective. keypad or keyboards take physical movements that the human user outputs and convert them into input signals that a mobile can understand; the output from these devices is the mobile’s input. Similarly, monitors or display take signals that a mobile outputs as input, and they convert these signals into a representation that human users can understand. From the human [user](https://en.wikipedia.org/wiki/User_(computing))'s perspective, the process of reading or seeing these representations is receiving output; this type of interaction between mobiles and humans is studied in the field of [human-mobiles interaction](https://en.wikipedia.org/wiki/Human%E2%80%93computer_interaction).

In computerand mobile architecture, the combination of the [CPU](https://en.wikipedia.org/wiki/Central_processing_unit) and [main memory](https://en.wikipedia.org/wiki/Main_memory), to which the CPU can read or write directly using individual [instructions](https://en.wikipedia.org/wiki/Instruction_(computer_science)), is considered the brain of a computer. Any transfer of information to or from the CPU/memory combo, for example by reading data from a [disk drive](https://en.wikipedia.org/wiki/Disk_drive), is considered I/O.[[1]](https://en.wikipedia.org/wiki/Input/output#cite_note-teco-1) The CPU and its supporting circuitry may provide [memory-mapped I/O](https://en.wikipedia.org/wiki/Memory-mapped_I/O) that is used in low-level [computer programming](https://en.wikipedia.org/wiki/Computer_programming), such as in the implementation of [device drivers](https://en.wikipedia.org/wiki/Device_driver), or may provide access to [I/O channels](https://en.wikipedia.org/wiki/Channel_I/O). An [I/O algorithm](https://en.wikipedia.org/wiki/External_memory_algorithm) is one designed to exploit locality and perform efficiently when exchanging data with a secondary storage device, such as a disk drive.

* **INTERFACE**

An I/O interface is required whenever the I/O device is driven by a processor. Typically a CPU communicates with devices via a [bus](https://en.wikipedia.org/wiki/Bus_(computing)). The interface must have necessary logic to interpret the device address generated by the processor. [Handshaking](https://en.wikipedia.org/wiki/Handshaking) should be implemented by the interface using appropriate commands (like BUSY, READY, and WAIT), and the processor can communicate with an I/O device through the interface. If different data formats are being exchanged, the interface must be able to convert serial data to parallel form and vice versa. Because it would be a waste for a processor to be idle while it waits for data from an input device there must be provision for generating [interrupts](https://en.wikipedia.org/wiki/Interrupt) and the corresponding type numbers for further processing by the processor if required.

A mobile that uses [memory-mapped I/O](https://en.wikipedia.org/wiki/Memory-mapped_I/O) accesses hardware by reading and writing to specific memory locations, using the same assembly language instructions that mobile would normally use to access memory. An alternative method is via instruction-based I/O which requires that a CPU have specialized instructions for I/O.Both input and output devices have a [data processing](https://en.wikipedia.org/wiki/Data_processing) rate that can vary greatly.With some devices able to exchange data at very high speeds [direct access](https://en.wikipedia.org/wiki/Direct_memory_access) to memory (DMA) without the continuous aid of a CPU is required.

**LEGAL INFORAMTION**

The wireless phone described in this guide is approved for use in GSM 900, 1800 and 1900 networks.

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Printed in Canada 02/2003.

US Patent No 5818437 and other pending patents.

T9 text input software

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Includes RSA BSAFE cryptographic or security protocol software fromRSA Security.

Java is a trademark of Sun Microsystems, Inc.

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Your phone may cause TV or radio interference (for example, when using a telephonein close proximity to receiving equipment). The FCC or Industry Canada can requireyou to stop using your telephone if such interference cannot be eliminated. If yourequire assistance, contact your local service facility. This device complies with part15 of the FCC rules. Operation is subject to the condition that this device does notcause harmful interference

**CERTIFICATE INFORMATION (SAR INFORMATION)**

THISMODELPHONEMEETSTHEGOVERNMENT'SREQUIREMENTSFOR EXPOSURE TO RADIOWAVES.

Yourwirelessphoneisaradiotransmitterandreceiver.Itisdesignedand manufacturednottoexceedtheemissionlimitsforexposuretoradio frequency(RF)energysetbytheFederalCommunicationsCommissionof theU.S.Government.Theselimitsarepartofcomprehensiveguidelines andestablishpermittedlevelsofRFenergyforthegeneralpopulation.The guidelinesarebasedonstandardsthatweredevelopedbyindependent scientificorganizationsthroughperiodicandthoroughevaluationof scientificstudies.Thestandardsincludeasubstantialsafetymargin designedtoassurethesafetyofallpersons,regardlessofageandhealth.

Theexposurestandardforwirelessmobilephonesemploysaunitof measurementknownastheSpecificAbsorptionRate,orSAR.TheSAR limitsetbytheFCCis1.6W/kg.\*TestsforSARareconductedusing standard operating positions accepted by the FCC with the phone transmittingatitshighestcertifiedpowerlevelinalltestedfrequency bands.AlthoughtheSARisdeterminedatthehighestcertifiedpower level,theactualSARlevelofthephonewhileoperatingcanbewellbelow themaximumvalue.Thisisbecausethephoneisdesignedtooperateat multiplepowerlevelssoastouseonlythepowerrequiredtoreachthe network.Ingeneral,thecloseryouaretoawirelessbasestationantenna, the lower the poweroutput.

Beforeaphonemodelisavailableforsaletothepublic,itmustbetested andcertifiedtotheFCCthatitdoesnotexceedthelimitestablishedby thegovernment-adoptedrequirementforsafeexposure.Thetestsare performedinpositionsandlocations... forexample,attheearandwornon thebodyasrequiredbytheFCCforeachmodel.ThehighestSARvalue forthismodelphoneasreportedtotheFCCwhentestedforuseatthe earis0.88W/kg,andwhenwornonthebody,asdescribedinthisuser guide,is1.21W/kg.Body-wornmeasurementsdifferamongphone models,dependinguponavailableaccessoriesandFCCrequirements

WhiletheremaybedifferencesbetweentheSARlevelsofvariousphones andatvariouspositions,theyallmeetthegovernmentrequirement

TheFCChasgrantedanEquipmentAuthorizationforthismodelphone withallreportedSARlevelsevaluatedasincompliancewiththeFCC RFexposureguidelines.SARinformationonthismodelphoneisonfile withtheFCCandcanbefoundundertheDisplayGrantsectionof [**http://www.fcc.gov/oet/fccid**](http://www.fcc.gov/oet/fccid)aftersearchingonFCCIDPPI**NPL**-**2**or PPI**NPL-2H**.

Forbodywornoperation,thisphonehasbeentestedandmeetstheFCC RFexposureguidelinesforusewithanaccessorythatcontainsnometal andthatpositionsthehandsetaminimumof5/8inch(1.5cm)fromthe body.UseofotheraccessoriesmaynotensurecompliancewithFCCRF exposureguidelines.Ifyoudonotuseabody-wornaccessoryandarenot holdingthephoneattheear,positionthehandsetaminimumof5/8inch (1.5cm)fromyourbodywhenthephoneisswitchedon.

\*IntheUnitedStatesandCanada,theSARlimitformobilephonesused bythepublicis1.6watts/kilogram(W/kg)averagedoveronegramof tissue.Thestandardincorporatesasubstantialmarginofsafetytogive additionalprotectionforthepublicandtoaccountforanyvariationsin measurements.SARvaluesmayvarydependingonnationalreporting requirementsandthenetworkband.ForSARinformationinotherregions pleaselookunderproductinformationat[**www.nokia.com/us**.](http://www.nokia.com/us)